Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM13UF0051E
EPC Gen2 UHF Tag Chip

Datasheet

Sept. 2023

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1 Description

FM13UF0051E (shorted to UF0051E) is an UHF Tag Chip IC developed by Fudan Microelectronics Company in accordance with EPC Global Class1 Gen2V2 and ISO/IEC 18000-63(TypeC).

Please contact Fudan Microelectronics Company to get more documents to support the detailed design and development.

2 Product Overview

2.1 Introduction

UF0051E is an UHF Tag Chip IC developed by Fudan Microelectronics Company. The chip is in accordance with EPC Global Class1 Gen2V2 and ISO/IEC 18000-63(TypeC).

With the industry-leading RF Performance, the UF0051E is particularly well suited for inventory management applications, supply chain management, personnel or vehicle identification, library management, airline luggage tracking, intelligent manufacturing and other fields.

2.2 Product Features

2.2.1 Contactless Interface

- EPC Global Class1 Gen2V2 & ISO/IEC 18000-63 compliant
- Frequence Range: 840~960MHz
- Anti-Collision
- Read sensitivity -24dBm
- Write sensitivity -23dBm
- Data rates:
  - Forward link 40~160Kbits/s
  - Reverse link 5~640Kbits/s

2.2.2 NVM Memory

- EPC memory: 160 bits
- User memory: 32 bits
- TID memory: 96bits
- Reserved memory: 64bits, include 32bits Access password and 32bits Kill password
- Endurance: 100,000 cycles
- Data retention: 50 years

2.2.3 Security Features

- 96-bit Unique Tag Identifier (TID), factory locked, read only
- Password verification function
- Lock command
- Kill command

2.2.4 Features

- Backscatter strength configurable
- Memory erase/write speed configurable
- Product Status Flag(PSF) function
- Parallel Encoding function
- Ultra reliable data reading function, invoid sending back wrong EPC, TID, or User data

- Fast Initialization mode

2.3 Function Block Diagram

UF0051E consists of three major blocks:

- Analog Part
- Digital Part
- NVM Memory

The analog part provides stable supply voltage harvested from the field and demodulates data received from the reader which is then transfered to the digital part. The modulation transistor of the analog part also transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the NVM memory.

The NVM memory contains the Reserved memory, TID, EPC and User memory.

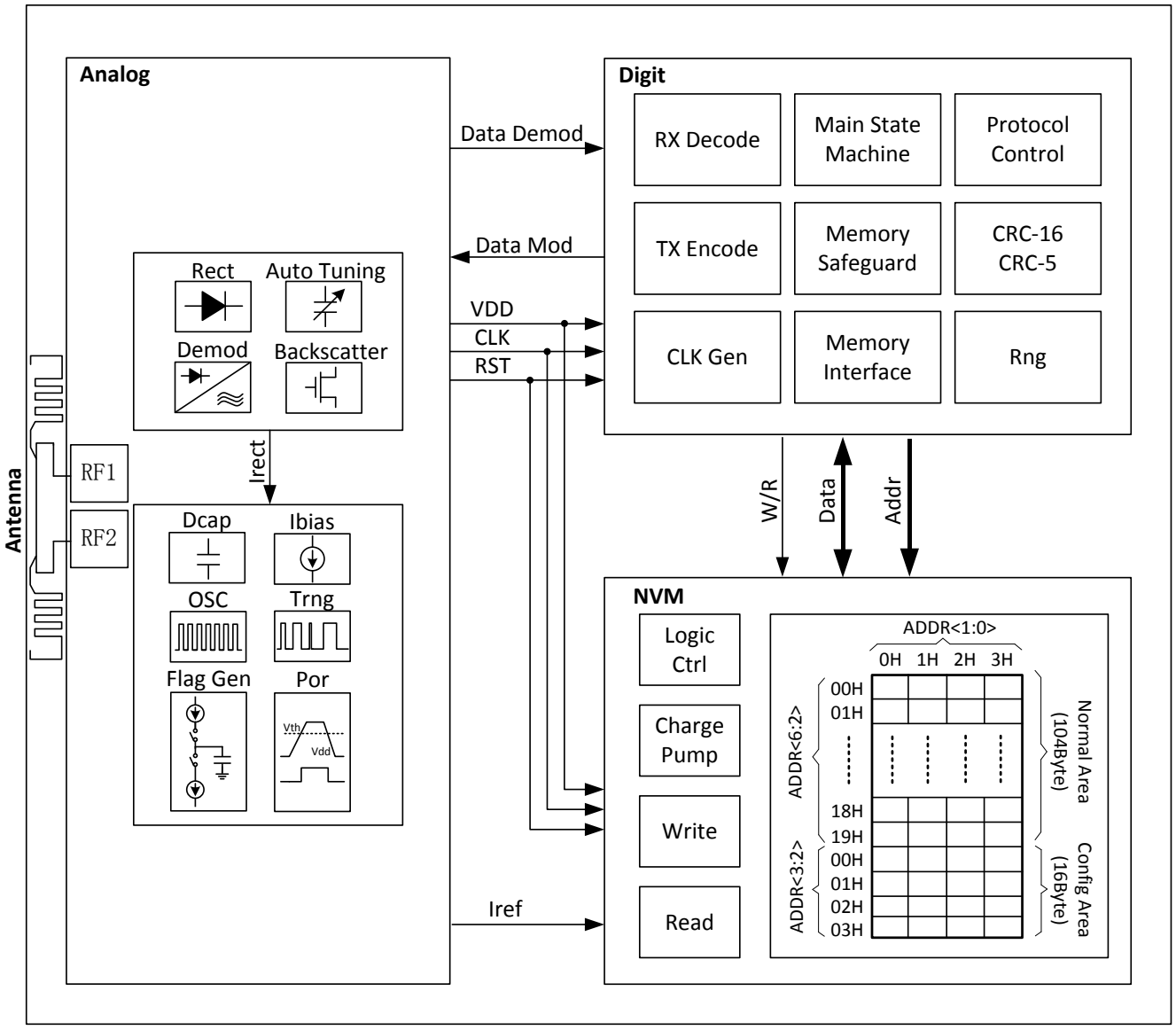


Figure 2-1 FM13UF0051E Block diagram

2.3.1 Pin Information

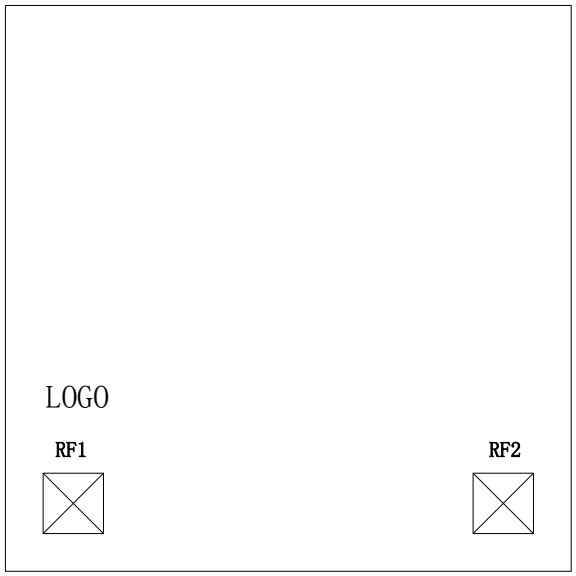


Figure 2-2 Pin assignment,Bumps

Table 2-1 Pin description, Bumps

Pin No.	Pin Name	Description
1	RF1	RF antenna connection pin
2	RF2	RF antenna connection pin

3 Function Description

3.1 Air Interface Standards

UF0051E supports the “EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Standard, Specification for RFID Air Interface Protocol for Communications at 860MHz – 960 MHz, Version 2.0.1”.

3.2 Data Transfer

3.2.1 Interrogator to Tag

An interrogator transmits information to UF0051E by modulating an UHF RF signal. UF0051E receives both information and operating energy from this RF signal. UF0051E are used as passive tags, meaning that all of their operating energy is received from the interrogator's RF field.

The interrogator should use a fixed modulation and data rate for the duration of one inventory round. It communicates to the UF0051E by modulating an RF carrier.

3.2.2 Tag to Interrogator

After a valid command transmision, the interrogator receives information from a UF0051E tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. UF0051E responds by switching the reflection coefficient of its antenna.

UF0051E communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

3.3 Command Set

3.3.1 Mandatory Commands

UF0051E supports all mandatory EPC Global Gen2V2 commands including:

– Kill

– Lock(can lock each memory independently,or lock all memory at once if payload is 0xFFFFF)

3.3.2 Optional Commands

The UF0051E also supports the following optional commands:

– Access

– BlockWrite (32 bits)

3.4 Memory

UF0051E's memory is logically separated into four distinct memory banks according to “EPC Global Class1 Gen2”. The memory banks are shown as below:

Bank Name	Bank Size	Bank
EPC	160 bits (including CRC-16 and PC)	01
User	32bits	11
TID	96bits	10
Reserved	64bits	00

The logical address of all the four memory banks begins at 00h.

One Configuration Word is available at EPC bank address bit 200h-20fh. The Configuration Word is described in detail in section 3.4.2.

3.4.1 Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	RESERVED	00h-0Fh	Kill Password[31:16]
		10h-1Fh	Kill Password[15:0]
		20h-2Fh	Access Password[31:16]
		30h-3Fh	Access Password[15:0]
01	EPC	00h-0Fh	CRC-16
		10h-1Fh	Protocol-Control Bits (PC)
		20h-2Fh	EPC[127:112]
		30h-3Fh	EPC[111:96]
		40h-4Fh	EPC[95:80]
		50h-5Fh	EPC[79:64]
		60h-6Fh	EPC[63:48]
		70h-7Fh	EPC[47:32]
		80h-8Fh	EPC[31:16]
		90h-9Fh	EPC[15:0]
		200h-20Fh	Configuration Word
10	TID	00h-0Fh	Allocation Class Identifier+Manufacturer ID
		10h-1Fh	Manufacturer ID+Model Number
		20h-2Fh	XTID_Header
		30h-3Fh	TID_Serial[47:32]
		40h-4Fh	TID_Serial[31:16]
		50h-5Fh	TID_Serial[15:0]
11	USER	00h-0Fh	WORD0[15:0]
		10h-1Fh	WORD1[15:0]

3.4.2 Configuration Word

The Configuration Word is located at address 200h-20fh of the EPC memory. Some functions of UF0051E can be activated or de-activated by changing the content of the corresponding bit in the Configuration Word. The change action will only take effect after a chip reset.

RFU：Reserved for Future Use

DTU：Don't Touch by Users

EPC Addr	Function Description	Default Value
200h	Write_Driver_Cfg: The configuration of the power driver during the NVM memory write cycle. When higher power driver is selected, the data writing to the NVM memory is more reliable. At the same time, more energy is needed from the RF field. 2'b00:Low; 2'b01:Medium; 2'b10:High	0
201h		1
202h	Parallel_Encoding 1'b1:Enable the Parallel Encoding function This bit can be set to 1 by a special Select command.	0
203h	DTU	0
204h	DTU	0
205h	Fast Initialization mode enable bit, if this bit is set to "1", the initialization function will be enabled. In this mode, if the initial content of the memory is all 0, the Write command's executing time will be shortten to the half of that in normal mode.	1
206h	RFU	0
207h	DTU	0
208h	DTU	0
209h	DTU	0
20Ah	DTU	0
20Bh	Backscatter strength configuration	0
20Ch		1
20Dh	Write_Time_Cfg: The configuration bits of the write time of the NVM memory 2'b00:0.6ms；2'b01:1.2ms；2'b10:2.4ms；2'b11:4.8ms	0
20Eh		1
20Fh	PSF alarm flag	0

3.4.2.1 Backscatter Strength Configuration

There are four backscatter strength modes for the UF0051E. The four modes can be controlled by modifying bit 20Bh and 20Ch within the configuration word. Normal backscatter(2'b01) is selected as the default.

The four backscatter strength modes are shown as below:

20Bh	20Ch	Backscatter Mode
0	0	Low Backscatter

20Bh	20Ch	Backscatter Mode
0	**1**	**Normal Backscatter (default)**
1	0	High Backscatter
1	1	Maximum Backscatter

3.4.2.2 Product Status Flag（PSF）

UF0051E provides a Product Status Flag(PSF) function, which can be used for EAS(Electronic Article Surveillance) implementations, Quality-Inspection or other related fields. PSF can be changed by modifying bit 20Fh of the configuration word.

The tags whose PSF is deactivated(PSF = 0) will not reply any future command after a special **Select** command,until the next power on. When PSF is activated (PSF = 1), the tags can still reply their EPC number after a custom **Select** command.

The special **Select** command is shown as below:

Name	Bits	Para Value	Description
CMD	4	1010b	Select command code
Target	3	001b	Fixed Value
Action	3	101b	Fixed Value
MemBank	2	01b	Fixed Value, 01b:EPC
Pointer	16	20Fh	Fixed Value, up to EVB's format
Length	8	01h	Fixed Value
Mask	1	1b	Fixed Value
Truncate	1	0b	Fixed Value
CRC	16	CRC-16	Calculated from the command parameters

3.4.3 TID

UF0051E’S TID is shown in below table. This memory is turned to read only in factory.

Class ID (8bits)	Mask Designer ID (12bits)	Model Number (12bits)	XTID (16bits)	Serial Number (48bits)
E2h	827h	802h/882h	2000h	SN

Model Number:
802h, data verification function is enabled. 882h, data verification function is disabled.

3.4.4 Initial Configuration

The initial data of UF0051E’s EPC bank is the same to that in TID except that XTID is 0000h.

User can change the content of EPC bank as they want.

E2h	827h	802h/882h	0000h	SN

The default value of Kill password and Access password in Reserved bank is all 0.
Except for TID bank, all of the banks in the chip are in un-locked state when it leaving factory.

3.4.5 Reliable read function

When the tag is in the farthest distance of the RF field or receives some interference signal, there will be an error in reading the content of the memory possibly. The reader will receive wrong data since it cannot judge it from the communication CRC verification. For example, there are 10 tags in the RF field, but the reader receives 12 EPC data in the inventory. This will lead to trouble for the application.
UF0051E has data verification function for every memory bank. During a typical inventory round, if an error is detected in the PC word or the EPC data, the tag will backscatter a zero-length EPC. If an error is detected during a READ command, the tag will response with the incorrect data and an inverted CRC. Reader can make strategy based on these information.

For example：

	Correct Data	Incorrect Data
Inventory	1400h_11223344h_30F9h *（PC _ EPC Data_CRC）*	0400h_2E34h *(PC _CRC)*
Read	3344h_3618h_316dh *(Data_Handle_CRC)*	33c4h_3618h_f5c8h *(Data_Handle_InvertedCRC)*

3.4.6 Fast Write Function

The speed of memory write operation affects the efficiency on the tag production line and the experience in user application. Several design is used to enhance the write speed and distance.

3.4.6.1 Configurable Write Speed

The write speed of UF0051E's memory can be configurated by changing the configuration bits in the EPC address 200h~201h which is related to the **write driven ability** and the EPC address 20Dh~20Eh which is the configuration of the **write time**. It aims to get faster write speed and better reliability.
The write driven ability is set to be stronger, the data is easier to be written into the memory. Accordingly, the write sensitivity is lower because more RF power is needed. So when the tag is moving in a certain speed, the time of the tag stays in the RF field will be shorten. On the contrary, if the driven ability is set to be weaker, although it is harder for writing data, the write sensitivity will be enhanced. Accordingly, the time of the tag stays in the RF field will be longer.

UF0051E provids low, medium and high driven ability configuration.

The write time is refer to the time that the tag needed to finish the data writting process. It is related to the environment temperature and the RF power that the tag receives. UF0051E provids 0.6ms, 1.2ms, 2.4ms and 4.8ms configuration options. User can do the selection based on their application situation. For example:

In the EPC data initialization process in the tag factory, if the environment and the field power is under controlled, the write time can be set to be shorter to enhance the production efficency.

When the tag is used in the actal application, if there is no high demand for the write speed, longer write time option can be selected. Meanwhile, the low driven ability option can be set to enhance the write sensitivity and make the operation distance longer.

3.4.6.2 Parallel Encoding

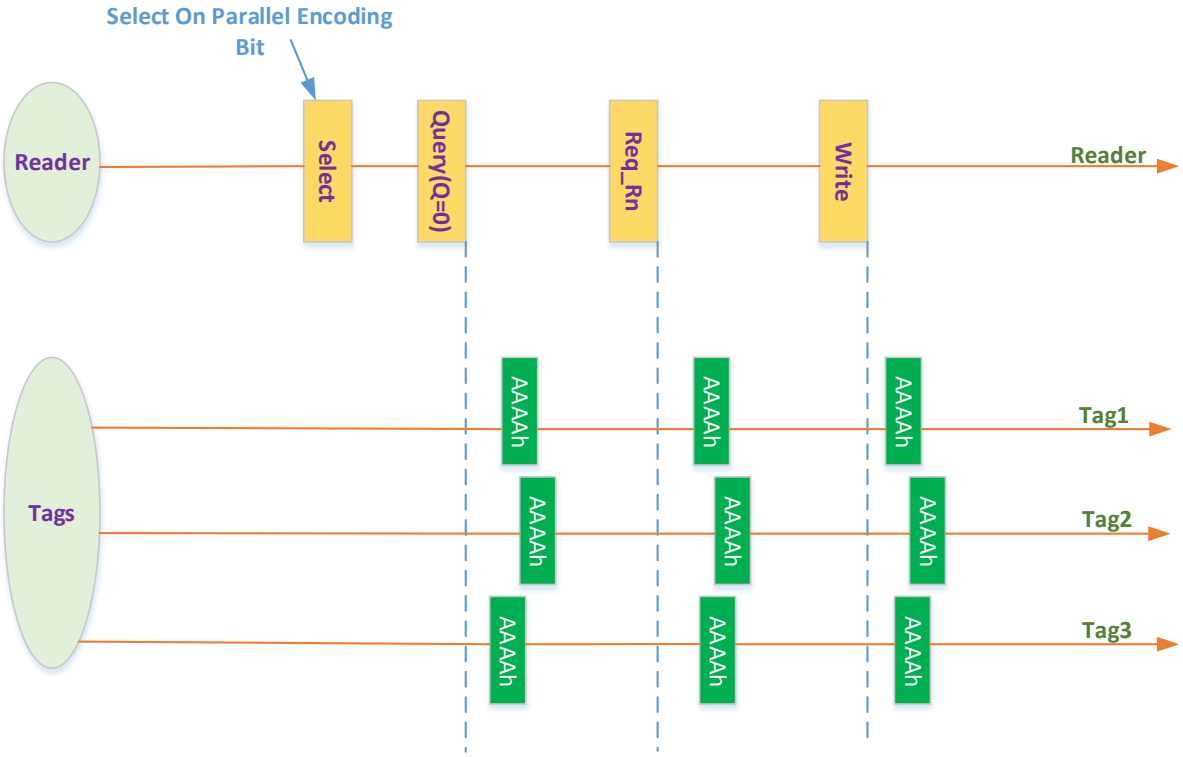
The Parallel Encoding function can be activated by setting the Parallel_Encoding enable bit to 1. The Parallel_Encoding enable bit is in the EPC bank at address 202h. This bit can be set to 1 by a special Select command. The command's format is as follows:

Name	Bits	Para Value	Description
CMD	4	1010b	Select command code
Target	3	xxxb	**Target** and **Action** should work together to ensure the current tag's flag has not been changed.
Action	3	xxxb	
MemBank	2	01b	Fixed Value, 01b:EPC
Pointer	16	202h	Fixed Value, up to EVB's format
Length	8	01h	Fixed Value
Mask	1	1b	Fixed Value
Truncate	1	0b	Fixed Value
CRC	16	CRC-16	Calculated from the command parameters

The Parallel-Encoding function works as follows:

- Activate the Parallel-Encoding function by a special **Select** command.
- The reader sends **Query** command to the tags. All the tags received the valid **Query** command reply fixed handle("AAAA"), then jump to the Open state.
- The reader can operate all the tags which is in Open state by **Write** command simultaniously. This will greatly save the time during multiple tags initializing.

Procedure of Parallel Encoding is shown as below:



The maximum amount of tags supported in a Parallel Encoding process depends on the strength of the reader's RF field.

During a Parallel Encoding process, all the tags will backscatter their ACK response at almost the same time. Some bit-collisions may be detected, the reader should ignore them.

3.4.6.3 Data fast initialization function

UF0051E has the data fast initialization function which can be enabled by set the configuration bit to "1" in the EPC address 205h.

After the function has been enabled, the chip will be in the fast initialization mode when the data is all "0" in the memory. Half of the time is needed to fulfill the write operation comparing with that in the normal mode. Since the initial data of the User bank is all "0", this function is useful when data is needed to be written to the User bank. The data initialization efficiency can be enhanced significantly.

Block Write command is recommended to be used in writting process.

4 Characteristics

4.1 Limiting Values

Table 4-1 Limiting parameters [1]

Symbol	Parameter	Min	Max	Unit
T_{stg}	Storage Temperature	-55	+125	°C
P_i	Max. Input Power	-	20	dBm
V_{ESD}	ESD（HBM）[2]	-	±2000	V
V_{ESD}	ESD（CDM）[3]	-	±200	V

[1]: Stresses above one or more of the limiting values may cause permanent damage to the device.
[2]: HBM:ANSI/ESDA/JEDEC JS-001-2017，the test chip has been mounted into a CDIP8 package.
[3]: CDM:ANSI/ESDA/JEDEC JS-002-2018，the test chip has been mounted into a CDIP8 package.

4.2 Normal Working Condition

Table 4-2 Normal working condition

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Temperature	-40	+25	+85	°C

4.3 Memory reliability

Table 4-3 Memory reliability

Symbol	Parameter	Conditions	min	typ	max	unit
t_{ret}	Data retention	T_{amb} = 55℃	50	-	-	year
$N_{endu(W)}$	Endurance	T_{amb} = 25℃	100,000	-	-	cycle

4.4 Electrical Characteristics

Table 4-4 Electrical characteristics

Symbol	Parameter	Conditiion	Min	Typ	Max	Unit
f_i	Operating Frequency Range	[1]	840	-	960	MHz
Pi（min）	Minimum Input Power	Read sensitivity 25℃ [2]	-	-24	-	dBm
Pi（min）	Minimum Input Power	Write sensitivity 25℃[3]	-	-22	-	dBm
T(ew)	Memory Write Time	-40℃~85℃ Fast Initialization mode [4] Write_Time_Cfg:2'b00 Write_Driver_Cfg: 2'b01 Write 32bits data by the BlockWrite command	-	0.6	-	ms
		-40℃~85℃ Fast Initialization mode [4] Write_Time_Cfg: 2'b01 Write_Driver_Cfg: 2'b01 Write 32bits data by the BlockWrite command	-	1.2	-	ms
		-40℃~85℃ Normal mode [4] Write_Time_Cfg: 2'b00 Write_Driver_Cfg: 2'b01 Write 32bits data by the BlockWrite command	-	1.2	-	ms
		-40℃~85℃ Normal mode [4] Write_Time_Cfg: 2'b01 Write_Driver_Cfg: 2'b01 Write 32bits data by the BlockWrite command	-	2.4	-	ms
C_p	Chip parallel capacitance	At minimum operating power, Large Pads	-	0.7	-	pF
R_p	Chip parallel resistance	At minimum operating power, Large Pads	-	5	-	kΩ
Z_i	Chip input impedance	915MHz At minimum operating power, Large Pads	-	12-j247	-	Ω

【1】: Bandwidth limitation according to ISM band regulations.
【2】: Tag sensitivity with a 2.15 dBi gain antenna
【3】: Tag sensitivity with a 2.15 dBi gain antenna, Write_Time_Cfg=2'b11,Write_Driver_Cfg=2'b00.
【4】: When the memory's initial content is all "0"，the chip works in Fast Initialization mode; When the memory content is not all "0"，the chip works in Normal mode.

5 Ordering Information

Device number	Package	Packing
FM13UF0051E-020-WTBU2-C	Bump Sawn Wafer	12 inch bump wafer (sawn, 120 um thickness, UV exposure, on film frame carrier)
FM13UF0051E-021-WTBU2-C	Bump Sawn Wafer	12 inch bump wafer (sawn, 120 um thickness, UV exposure, on film frame carrier)

FM 13UF 005 1E - XXX - XXXXX - X

Company name prefix

FM: Shanghai Fudan Microelectronics

Product family

13UF: UHF tag chip

Product Memory

005: about 0.5Kbits

Product version

1: First Gen

E: EPC Gen and ISO18000-63 (Type C) compliant

Model Number

020：data verification function is enabled.

021：data verification function is disabled.

Package

WTBU2: Bump Wafer

Packing Code

C: sawn wafer packing

Revision History

Rev	Release date	Pages	Modifications
1.0	Mar. 2023	22	Initial Release Version.
1.1	Jun. 2023	22	In sections 3.4.3 and 3.4.4, add Model Number 882h and related descriptions. In section 3.4.5.1, modify the description of the Reliable Read function.
1.2	Aug. 2023	21	Fix clerical errors.
1.3	Sept. 2023	21	In section 4.4, modify the electrical characteristics, including write sensitivity, chip parallel capacitance, and chip input impedance.

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