400G QSFP56-DD SR8 Transceiver

Product Specifications

DATA SHEET
UCQ4HSR
400Gb/s QSFP56-DD SR8 70–100m, MMF, 850nm, MPO Transceiver

The Univiso 400G QSFP-DD SR8 Transceiver is designed to transmit and receive serial optical data links up to 8 x 53 .125Gbps data rate by PAM4 modulation format over multi-mode fiber.

Features

- Up to 53.125Gbps data rate per channel by PAM4 modulation
- Support 400GAUI-8 electrical interface
- Integrated 850nm VCSEL array and PD array
- Single MPO16 connector receptacle optical interface compliant
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Maximum power consumption 8W
- Single +3.3V power supply
- Reach up to 70m on MMF(OM3)
- Reach up to 100m on MMF(OM4)
- Compliant with ROHS2.0

Applications

•Data centers and Cloud Networks
•400GE Interconnect Requirements.

Standards

•IEEE 802.3cd
•QSFP-DD MSA
•CMIS4.0

Rev	Date	Modified by	Description
A	Sep 5,2021	Alan	Initial Release

1. Absolute Maximum Ratings

Product	Electrical mode	Protocol	Nominal Rate			Specifications	
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER
400G-SR8	8X50	IEEE802.3cd	425	26.5625 PAM4	±100	400GAUI-8	2.4E-4

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	RH	0	85	%

2. Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	℃	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Power Consumption	Pc	W		7.5	8

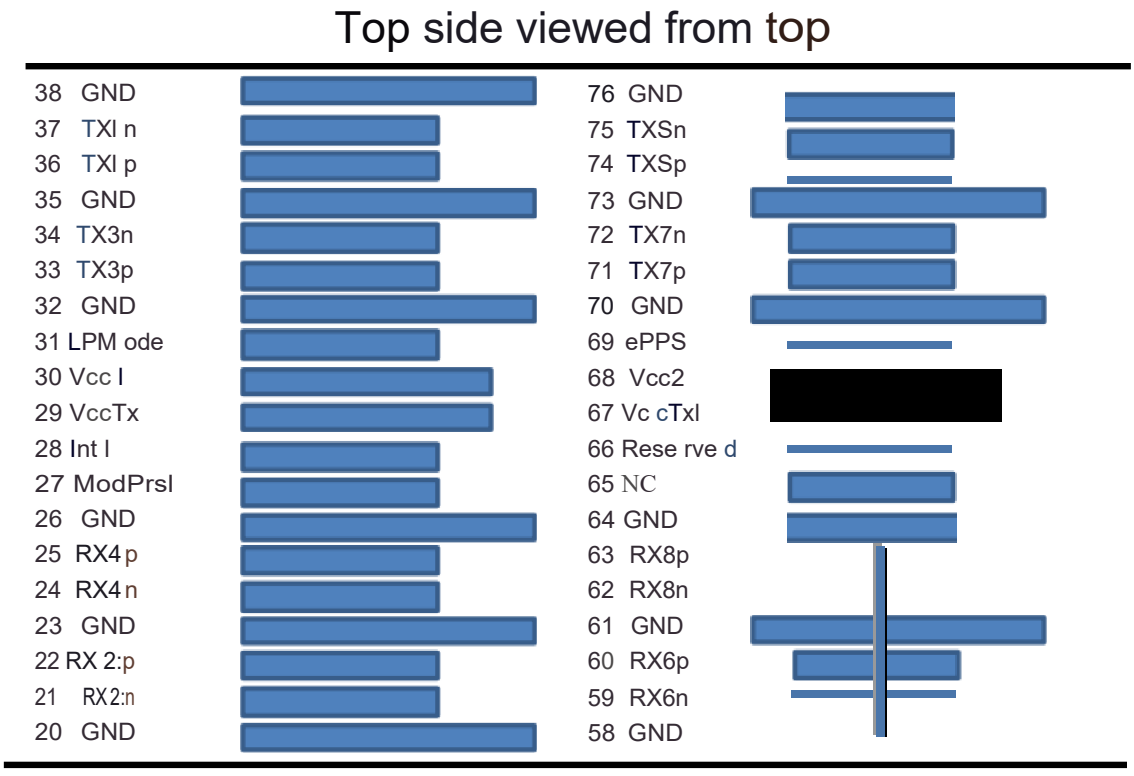
3. Transmitter characteristics

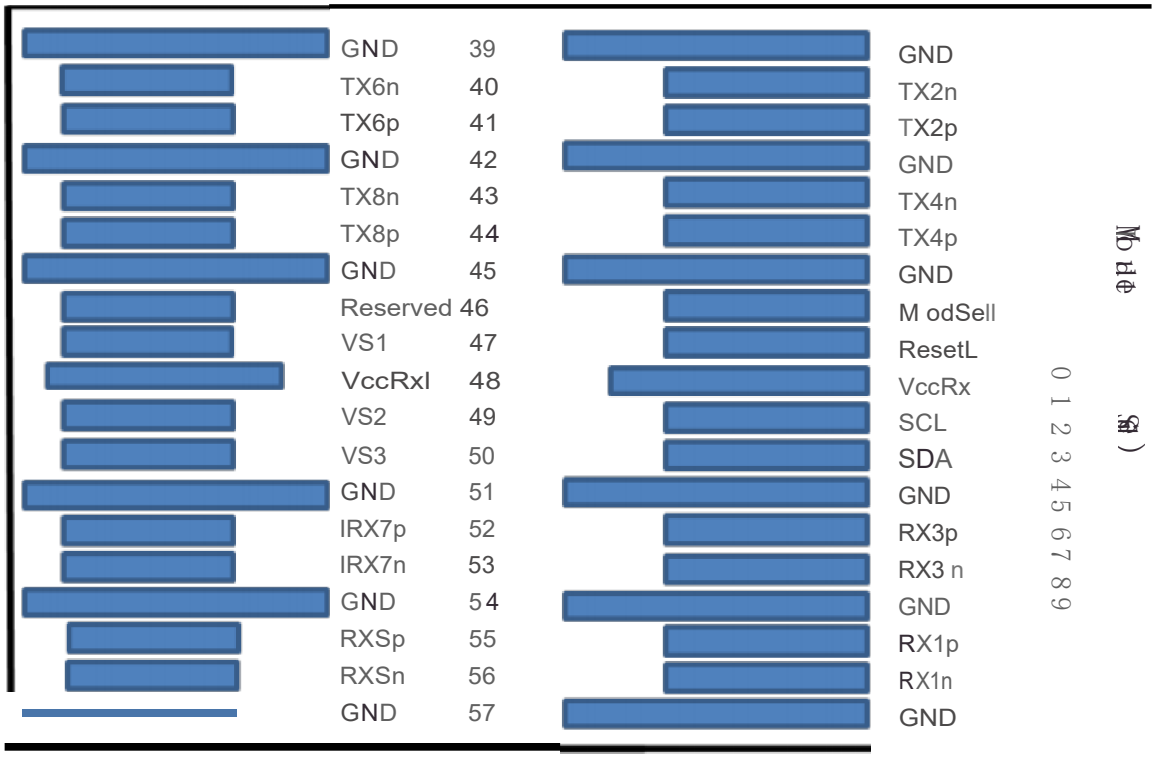
Parameter	Min	Typical	Max	Unit
Signaling Rate, each lane (range)	26.5625±100ppm			GBd
Center Wavelength Range	840		860	nm
Modulation Format	PAM4			
RMS spectral width			0.6	nm
Average launch power, each lane	-6.5		4	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane	-4.5		3	dBm
Launch power in OMAouter minus TDECQ	-5.9			dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			4.5	dB
Extinction ratio, each lane	3			dB
Optical return loss tolerance			12	dB
Encircled flux	≥86% at 19um ≤30% at 4.5um			

4. Receiver characteristics

Parameter	Min	Typical	Max	Unit
Signaling Rate, each lane (range)	26.5625±100ppm			GBd
Center Wavelength Range	840		860	nm
Modulation Format	PAM4			
Average receive power, each lane	-8.4		4	dBm
Receive power, each lane (OMAouter)			3	dBm
Receiver reflectance			-12	dB
Stressed receiver sensitivity (OMAouter), each lane			-3.4	dBm
Receiver sensitivity (OMAouter), each lane	Max(-6.5, SECQ-7.9)			dBm
Receiver Damage Threshold, each lane			5	dBm
Stressed eye closure for PAM4 (SECQ), lane under test		4.5		dB
SECQ – 10log10(Ceq) (max), lane under test			4.5	dB

5. Pin Description





Pad	Logic	Symbol	Description	Plug Sequence4	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data output	3B	
15	CML-O	Rx3n	Receiver Inverted Data output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.JV Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence	Notes
39		GND	Ground	1A	1
40	CML-I	Tx 6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx 6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx 8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx 8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VSl	Module Vendor Specificl	3A	3
48		VccRxl	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receivre Non-Inverted Data output	3A	
56	CML-O	Rx5n	Receiver Inverted Data output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTxl	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx Sp	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx Sn	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRxl, Vccl, Vcc2, VccTx and VccTxl shall be applied concurrently. Requirements defined for the host side of the Host card Edge Connector are listed in Table 7. VccRx, VccRxl, Vccl, Vcc2, VccTx and VccTxl may be internally connected within the module in any combination. The connector Vee pins are each rated for a maximum current of 1000 mA.

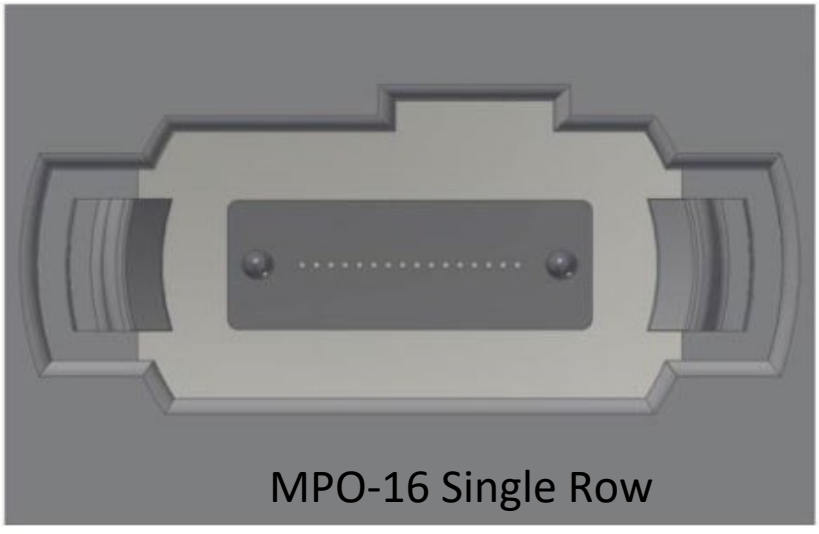
Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhrns and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

6. Module Memory Map

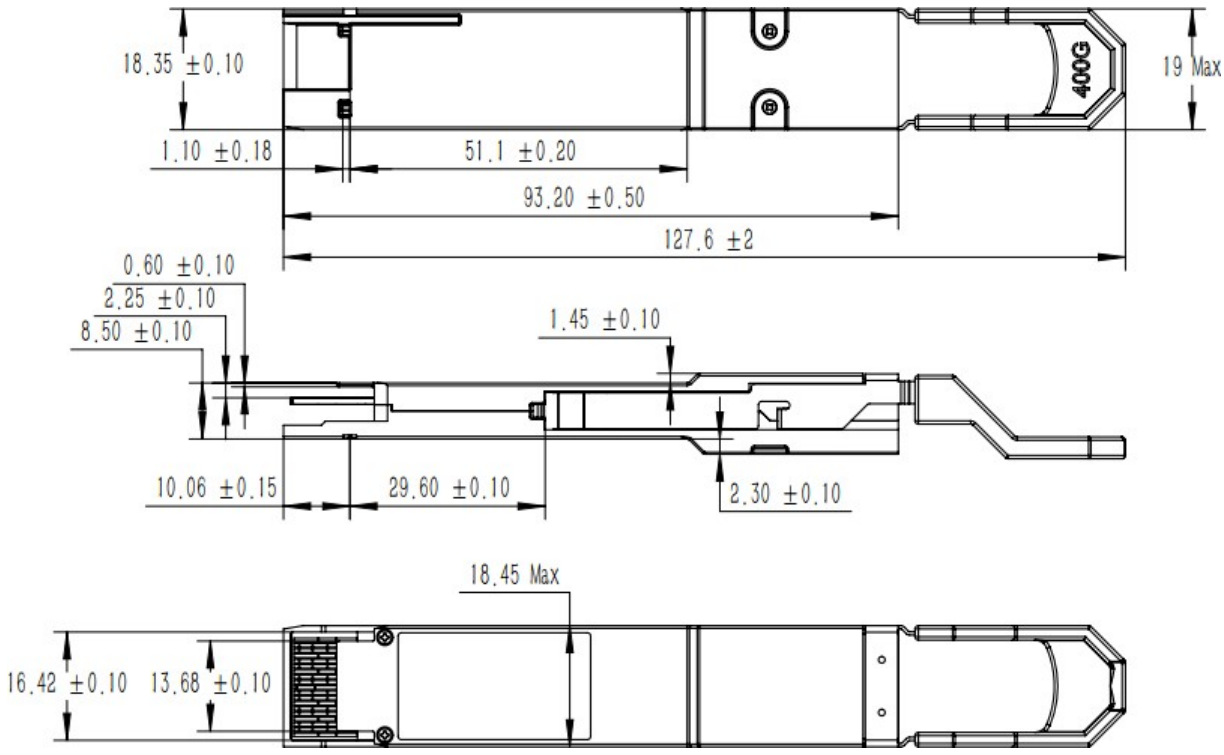
Compatible with QSFP-DD CMIS rev 4.0

7. Optical interface



8. Package Outline

Compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



9. Order information

Part Number	Description
UCQ4HSR	400G QSFP56-DD SR8 Transceiver

XX: customized; 01 means Univiso standard product