# DATA SHEET

UMQ40L2L

## 40Gb/s QSFP+ LR4 Optical Transceiver

## QSFP10-LR4-D12 Overview

UNIVISO's QSFP+ LR4 optical transceivers are based on Ethernet IEEE 802.3ba
standard and SFF 8436 standard. The QSFP+ transceiver transmitter converts 4 input 10Gb/s electrical data paths to 4 CWDM optical paths and multiplexes them into a single 40Gb/s optical transmission. To the receiver, the module optically de-multiplexes a 40Gb/s input optical signal into 4 CWDM optical signals, and converts them to 4 output electrical data paths. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm.

## Product Features

- Uncooled 4x10Gb/s CWDM transmitter
- Up to 10.3125Gbps data rate per wavelength
- QSFP+ MSA compliant
- Duplex LC connector
- Built-in digital diagnostic functions
- Up to 10km on SMF
- Maximum 2.5W power consumption
- RoHS Compliant
- Operating temperature range:$0°C$ to $70°C$
- XLPPI electrical interface
- Anti-sulphuration

## Applications

- 40G Ethernet

## Ordering Information

| Part Number | Description | Color on Clasp |
|---|---|---|
| UMQ40L2L | 40G QSFP+ LR4 LC Connectors, Up to 10km on SMF, with DOM function, Anti-sulphuration | Blue |
|  |  |  |

## General Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Bit Error Rate | BER |  |  | $10^{-12}$ |  |  |
| Operating Temperature | $T_C$ | 0 |  | 70 | $^\circ$C | 1 |
| Storage Temperature | $T_{STO}$ | -40 |  | 85 | $^\circ$C | 2 |
| Input Voltage | $V_{CC}$ | 3.14 | 3.3 | 3.46 | V |  |
| Maximum Supply Voltage | $V_{MAX}$ | -0.5 |  | 3.6 | V | 3 |

**Notes:**

1. Case temperature
2. Environment temperature
3. Electrical interface

## Link Distances

| Data Rate | Fiber Type | Link length supported (km) |
|---|---|---|
| 40 Gb/s | 50/125um OM3 MMF | 0.15 |
| 40 Gb/s | 50/125um OM4 MMF | 0.15 |
| 40 Gb/s | 9/125um SMF | 10 |

## Optical – Characteristics – Transmitter

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Total Average Launch Power | $P_{OUT}$ | | | 8.3 | dBm | |
| Average Launch Power per Lane | $TXP_x$ | -7 | | 2.3 | dBm | |
| Optical Center Wavelength(L0 Lane) | $\lambda_C$ | 1264.5 | 1271 | 1277.5 | nm | |
| Optical Center Wavelength(L1 Lane) | $\lambda_C$ | 1284.5 | 1291 | 1297.5 | nm | |
| Optical Center Wavelength(L2 Lane) | $\lambda_C$ | 1304.5 | 1311 | 1317.5 | nm | |
| Optical Center Wavelength(L3 Lane) | $\lambda_C$ | 1324.5 | 1331 | 1337.5 | nm | |
| Optical Modulation Amplitude | OMA | -4 | | 3.5 | dBm | |
| Extinction Ratio | ER | 3.5 | 5.0 | | dB | |
| Side Mode Suppression Ratio | SMSR | 30 | | | dB | |
| Relative Intensity Noise | RIN | | | -128 | dB/Hz | |
| Transmitter Dispersion Penalty | TDP | | | 2.6 | dB | |
| Optical Return Loss Tolerance | TOL | | | 20 | dB | |
| Transmitter eye mask definition | Compliant with IEEE 802.3ba standard | | | | | |
| Average launch power of OFF transmitter, per lane | | | | -30 | dBm | |

## Optical – Characteristics – Receiver

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|-----------|--------|-----|-----|-----|------|---------|
| Optical Center Wavelength (L0 Lane) | $\lambda_C$ | 1264.5 | 1271 | 1277.5 | nm | |
| Optical Center Wavelength (L1 Lane) | $\lambda_C$ | 1284.5 | 1291 | 1297.5 | nm | |
| Optical Center Wavelength (L2 Lane) | $\lambda_C$ | 1304.5 | 1311 | 1317.5 | nm | |
| Optical Center Wavelength (L3 Lane) | $\lambda_C$ | 1324.5 | 1331 | 1337.5 | nm | |
| Average Receive Power per Lane | $RXP_x$ | -13.7 | | 2.3 | dBm | |
| Damage Threshold per Lane | $P_{MAX}$ | 3.4 | | | dBm | |
| Receiver Sensitivity (OMA) per Lane | $RX_{sens}$ | | -14.0 | -11.5 | dBm | |
| Return Loss | RL | | | -26 | dB | |
| LOS Assert | $LOS_A$ | -28 | | | dBm | 1 |
| LOS De-Assert | $LOS_D$ | | | -15 | dBm | 1 |
| LOS Hysteresis | $LOS_H$ | 1 | 3 | | dB | |

**Notes:**
1. Average receive power.

## Electrical – Characteristics – Transmitter

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Input differential impedance | $R_{IN}$ | | 100 | | $\Omega$ | |
| Differential data input swing | $V_{IN\_PP}$ | 120 | | 1200 | mV | |
| Transmitter Disable Voltage | $V_{DIS}$ | $V_{CC}$-1.3 | | $V_{CC}$ | V | |
| Transmitter Enable Voltage | $V_{EN}$ | $V_{EE}$ | | $V_{EE}$+0.8 | V | |

## Electrical – Characteristics – Receiver

| Parameter | Symbol | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Differential data output swing | $V_{OUT\_PP}$ | 200 | | 400 | mV | 1, 2 |
| | | 300 | | 600 | mV | |
| | | 400 | 550 | 800 | mV | |
| | | 600 | | 1200 | mV | |
| Data output rise/fall time (20%-80%) | $t_r/t_f$ | 28 | | | ps | |
| LOS Fault Voltage | $V_{LOS\_A}$ | $V_{CC}$-1.3 | | $V_{CC\_HOST}$ | V | |
| LOS Normal | $V_{LOS\_D}$ | $V_{EE}$ | | $V_{EE}$+0.5 | V | |

**Notes:**
1. AC coupled with 100Ω differential output impedance.
2. Output voltage is settable in 4 discrete steps via I2C. Default is 400 - 800 mV.

## TX1-TX4 Typical Eye Pattern

Test Condition：30°C，BIAS=32-38mA
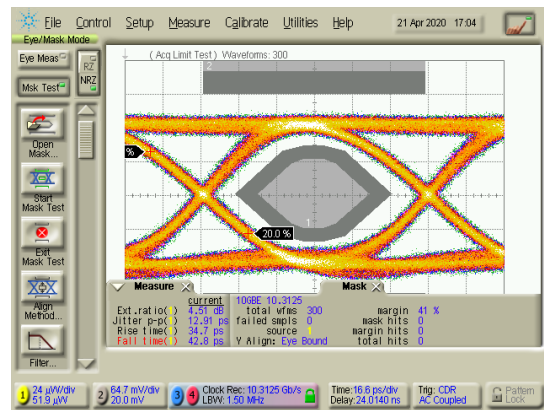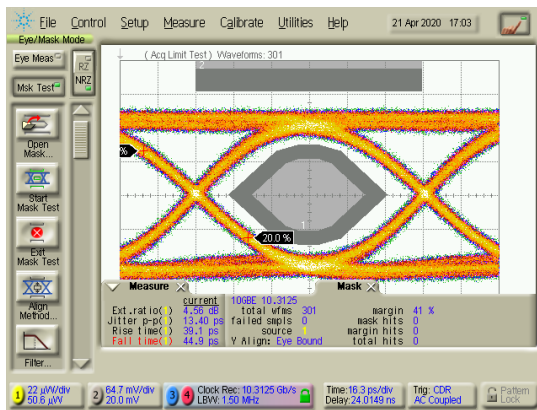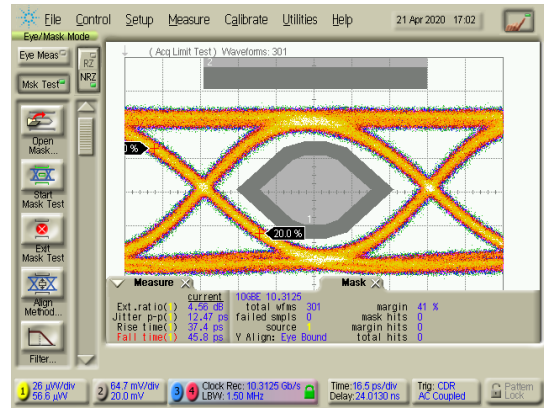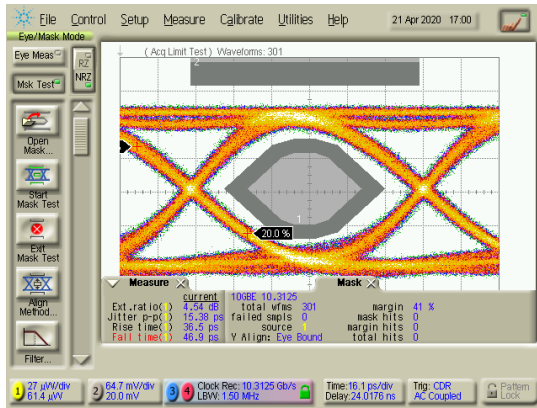
## A0H Lower Page 00h Register Map

| Memory Map(2-Wire Serial Address 1010000xb, Lower Page 00h) | | | | | |
|---|---|---|---|---|---|
| **IIC Addr** | **Size** | **Name** | **Description** | **Type** | **Value (HEX)** |
| 0 | 1 | Identifier | QSFP+ | R | 0D |
| 1 | 1 | Revision Compliance | SFF-8636 Rev2.10 | R | 08 |
| 2 | 1 | status | Bit 2 = 0b: Paging (at least upper page 03h implemented)<br>Bit 1 = 1b: IntL not asserted<br>Bit 0 = 0b: valid data can be read | R | 02 |
| 3 | 1 | Interrupt Flags (Clear on read) | Bit 7-4: Latched Tx4 - Tx1 LOS indicator<br>Bit 3-0: Latched Rx4 - Rx1 LOS indicator | R | 00 |
| 4 | 1 | Interrupt Flags (Clear on read) | Bit 7-4: Latched Tx4 - Tx1 input Adaptive EQ fault indicator, not implement<br>Bit 3-0: Latched Tx4 - Tx1 Transmitter/Laser fault indicator | R | 00 |
| 5 | 1 | Interrupt Flags (Clear on read) | Bit 7-4: Latched Tx4 - Tx1 CDR LOL indicator, not implement<br>Bit 3-0: Latched Rx4 - Rx1 CDR LOL indicator, not implement | R | 00 |
| 6 | 1 | Interrupt Flags (Clear on read) | Bit 7-4: Latched abnormal temperature indicator, include alarm and/or warning<br>Bit 1: TC readiness flag, not implement<br>Bit 0: Initialization complete flag, value is 0b means nitialization and/or reset has completed. | R | 00 |
| 7 | 1 | Interrupt Flags | Bit 7-4: Latched abnormal supply voltage indicator, include alarm and/or warning | R | 00 |
| 8 | 1 | Vendor Specific | Initialize to 00(hex) | R | |
| 9-10 | 2 | Interrupt Flags (Clear on read) | Latched abnormal Rx Power voltage indicator, include alarm and/or warning | R | 0000 |
| 11-12 | 2 | Interrupt Flags (Clear on read) | Latched abnormal Tx Bias current indicator, include alarm and/or warning | R | 0000 |
| 13-14 | 2 | Interrupt Flags (Clear on read) | Latched abnormal Tx Power voltage indicator, include alarm and/or warning | R | 0000 |
| 15-18 | 4 | Reserved | Initialize to 00(hex) | R | |
| 19-21 | 3 | Vendor Specific | Initialize to 00(hex) | R | |

| | | | | | |
|---|---|---|---|---|---|
| 22-23 | 2 | Temperature | Temperature diagnosis, LSB is 1/256 °C | R | |
| 24-25 | 2 | Reserved | Initialize to 00(hex) | R | |
| 26-27 | 2 | Supply Voltage | Supply Voltage diagnosis, LSB is 100 uV | R | |
| 28-29 | 2 | Reserved | Initialize to 00(hex) | R | |
| 30-33 | 4 | Vendor Specific | Initialize to 00(hex) | R | |
| 34-35 | 2 | Rx1 Power | Rx1 average receive power diagnosis, LSB is 0.1 uW | R | |
| 36-37 | 2 | Rx2 Power | Rx2 average receive power diagnosis, LSB is 0.1 uW | R | |
| 38-39 | 2 | Rx3 Power | Rx3 average receive power diagnosis, LSB is 0.1 uW | R | |
| 40-41 | 2 | Rx4 Power | Rx4 average receive power diagnosis, LSB is 0.1 uW | R | |
| 42-43 | 2 | Tx1 Bias | Tx1 bias current diagnosis, LSB is 2 uA | R | |
| 44-45 | 2 | Tx2 Bias | Tx2 bias current diagnosis, LSB is 2 uA | R | |
| 46-47 | 2 | Tx3 Bias | Tx3 bias current diagnosis, LSB is 2 uA | R | |
| 48-49 | 2 | Tx4 Bias | Tx4 bias current diagnosis, LSB is 2 uA | R | |
| 50-51 | 2 | Tx1 Power | Tx1 average launch power diagnosis, LSB is 0.1 uW | R | |
| 52-53 | 2 | Tx2 Power | Tx2 average launch power diagnosis, LSB is 0.1 uW | R | |
| 54-55 | 2 | Tx3 Power | Tx3 average launch power diagnosis, LSB is 0.1 uW | R | |
| 56-57 | 2 | Tx4 Power | Tx4 average launch power diagnosis, LSB is 0.1 uW | R | |
| 58-73 | 16 | Reserved | Initialize to 00(hex) | R | |
| 74-81 | 8 | Vendor Specific | Initialize to 00(hex) | R | |
| 82-85 | 4 | Reserved | Initialize to 00(hex) | R | |
| 86 | 1 | Tx Disable | Bit 3-0: Tx4 - Tx1 Disable, wtite 1b to close corresponding channel laser | R/W | 00 |
| 87 | 1 | Rx Rate select | Rx software rate select, not implement, fixed 10G mode | R/W | 00 |
| 88 | 1 | Tx Rate select | Tx software rate select, not implement, fixed 10G mode | R/W | 00 |
| 89-92 | 4 | Reserved | Initialize to 00(hex) | R/W | |

| 93 | 1 | Control | Bit 7: Software reset is a self-clearing bit, write 1b to trigger a module reset<br><br>Bit 1: Power set, write 1b to enable Low Power Mode, the module power consumption is lower than 1.5W | R/W | 00 |
|---|---|---|---|---|---|
| 94-97 | 4 | Reserved | Initialize to 00(hex) | R/W | |
| 98 | 1 | TX/RX CDR Control | module doesn't have CDR circuit, not implement. Initialize to 00(hex) | R/W | 00 |
| 99 | 1 | Control | Bit 1: LPMode/TxDis input signal control, not implement<br><br>Bit 0: IntL/LOSL output signal control, not implement | R/W | 00 |
| 100 | 1 | Mask | Bit 7-4: Masking bit for Tx4 - Tx1 LOS indicator<br><br>Bit 3-0: Masking bit for Rx4 - Rx1 LOS indicator | R/W | 00 |
| 101 | 1 | Mask | Bit 7-4: Masking bit for Tx4 - Tx1 Adaptive EQ fault, not implement<br><br>Bit 3-0: Masking bit for Tx4 - Tx1 Transmitter fault | R/W | 00 |
| 102 | 1 | Mask | Bit 7-4: Masking bit for Tx4 - Tx1 CDR Loss of Lock, not implement<br><br>Bit 3-0: Masking bit for Rx4 - RX1 CDR Loss of Lock, not implement | R/W | 00 |
| 103 | 1 | Mask | Bit 7-4: Masking bit for temperature abnormal indicator, include alarm and/or warning<br><br>Bit 1: Masking bit for TC readiness flag, not implement | R/W | 00 |
| 104 | 1 | Mask | Bit 7-4:Masking bit for Vcc abnormal indicator, include alarm and/or warning | R/W | 00 |
| 105-106 | 2 | Vendor Specific | Initialize to 0001(hex) | R/W | 0001 |
| 107 | 1 | Max Power Consumption | Maximum power consumption of module, LSB is 0.1 W | R | 19 |
| 108-109 | 2 | Propagation Delay | propagation delay, not implement | R | 00 |
| 110 | 1 | Free Side Device Properties | not implement | R | 00 |
| 111-112 | 2 | use by PCI Express | PCI Express relevant Specification,not implement | R/W | 0000 |

| 113 | 1 | Far-End and Near-End Implementation | Bit 6-4: Far-End Implementation,not implement<br>Bit 3-0: Near-End Implementation, not implement | R | 00 |
|---|---|---|---|---|---|
| 114 | 1 | use by microQSFP | microQSFP MSA function, not implement | R | 00 |
| 115-116 | 2 | Reserved | not implement | R | 0000 |
| 117-118 | 2 | Reserved | not implement | R/W | 0000 |
| 119-122 | 4 | Password Change Entry | Rewrite the fixed side manufacturer passwords entry, set to 00000000(hex) on power-up. The 4 bytes are write-only, read result always be 00(hex) | W | 00000000 |
| 123-126 | 4 | Password Entry | Write password to enter fixed or free side device mode. Set to 00000000(hex) on power-up. The 4 bytes are write-only, read result always be 00(hex) | W | 00000000 |
| 127 | 2 | Page Select | Select the upper page, for example write 02(hex) indicates upper memory Page 02h is mapped | R/W | 00 |

## A0 Wtite Protection

The module implement write protection of upper Page 00h and 02h of 2-Wire Serial Address 1010000x (A0 Device). User must enter the fixed side mode, if you want to rewrite the upper Page 00h and 02h area register data. The way to enter the fixed side mode is enter the default fixed mode password, 00001011(hex), to registers 123-126 of A0 device.

In this Version, fixed side system manufacturer passwords can be changed by writing a new password in Bytes 119-122 when the correct current fixed side manufacture password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password.

## A0H Upper Page 00h Register Map

| Memory Map(2-Wire Serial Address 1010000xb, Upper Page 00h) | | | | | |
|---|---|---|---|---|---|
| IIC Addr | Size | Name | Description | Type | Value (HEX) |
| 128 | 1 | Identifier | QSFP+ | R | 0D |
| 129 | 1 | Ext. Identifier | Power Class 3 (2.5 W max.), No CLEI code present in Page 02h, No CDR in Tx and Rx | R | 80 |
| 130 | 1 | Connector Type | Dual-LC (Lucent Connector) | R | 07 |
| 131-138 | 8 | Specification Compliance | 40GBASE-LR4, Long distance (L), Longwave laser (LC), Single Mode (SM) | R | 02000000 10100100 |
| 139 | 1 | Encoding | 64B/66B | R | 05 |
| 140 | 1 | Singaling rate,nominal | Unit is 100 Megabaud | R | 67 |
| 141 | 1 | Extended Rate Select Compliance | Rate select is not implement | R | 00 |
| 142 | 1 | Length (SMF) | Unit is kilometers | R | 0A |
| 143 | 1 | Length (OM3 50um) | Unit is 2 meters | R | 4B |
| 144 | 1 | Length (OM2 50um) | Unit is 2 meters | R | 00 |
| 145 | 1 | Length (OM1 62.5um) | Unit is 1 meter | R | 00 |
| 146 | 1 | Length (OM4 50um) | Unit is 2 meters | R | 4B |
| 147 | 1 | Device technology | 1310nm DFB, No wavelength control, Uncooled transmitter device, Pin detector, Transmitter not tunable | R | 40 |
| 148-163 | 16 | Vendor name | UNIVISO | R | ASCII Format |
| 164 | 1 | Extended Module | Do not support Infiniband application | R | 00 |
| 165-167 | 3 | Vendor OUI | IEEE Company Identifier for the vendor | R | 000000 |
| 168-183 | 16 | Vendor PN | Vendor Part Number | R | ASCII Format |
| 184-185 | 2 | Vendor rev | Vendor Part Revision Number | R | ASCII Format |
| 186-187 | 2 | Wavelength | Unit is 0.05nm | R | 666C |
| 188-189 | 2 | Wavelength tolerance | Unit is 0.005nm | R | 0514 |
| 190 | 1 | Max case temp. | Unit is °C | R | 46 |

| 191 | 1 | CC_BASE | The check code of bytes from 128 to 190 | R | |
| 192 | 1 | Link codes | Reserved | R | 00 |
| 193-195 | 3 | Options | Tx input equalizers, Rx output emphasis, or Rx output amplitude fixed-programmable settings is implemented. Tx/Rx Squelch Disable is implemented. Tx Squelch is implemented. Memory Page 02 provided. Tx_Disable is implemented. | R | 070B90 |
| 196-211 | 16 | Vendor SN | Vendor part Serial Number | R | ASCII Format |
| 212-219 | 8 | Date Code | Vendor's date code of production | R | ASCII Format |
| 220 | 1 | Diagnostic Monitoring Type | Temperature, supply voltage, received average power and transmitter average power monitoring are implemented. | R | 3C |
| 221 | 1 | Enhanced Options | Initialization Complete Flag and software reset are implemented | R | 11 |
| 222 | 1 | Baud Rate,nominal | Unit is 250 MBd. | R | 00 |
| 223 | 1 | CC_EXT | The check code of bytes from 192 to 222 | R | |
| 224-255 | 32 | Vendor Specific | Vendor Specific information | R | |

## A0H Upper Page 02h Register Map

| Memory Map(2-Wire Serial Address 1010000xb, Upper Page 02h) | | | | | |
|---|---|---|---|---|---|
| IIC Addr | Size | Name | Description | Type | Value (HEX) |
| 128-255 | 128 | user-writable EEPROM | The fixed side can read or write this memory for any purpose. | R | |

**Notes：**

1.The value of A0H Upper Page 00h and 02h Register Map is general version. The actual data written may be changed due to user compatibility without prior notice.

## A0H Upper Page 03h Register Map

| Memory Map(2-Wire Serial Address 1010000xb, Upper Page 03h) | | | | | |
|---|---|---|---|---|---|
| IIC Addr | Size | Name | Description | Type | Value (HEX) |
| 128-129 | 2 | Temp High Alarm | Value is 80°C | R | 5000 |
| 130-131 | 2 | Temp Low Alarm | Value is -10°C | R | F600 |
| 132-133 | 2 | Temp High Warning | Value is 75°C | R | 4B00 |
| 134-135 | 2 | Temp Low Warning | Value is -5°C | R | FB00 |
| 144-145 | 2 | Vcc High Alarm | Value is 3.7V | R | 9088 |
| 146-147 | 2 | Vcc Low Alarm | Value is 2.9V | R | 7170 |
| 148-149 | 2 | Vcc High Warning | Value is 3.6V | R | 8C70 |
| 150-151 | 2 | Vcc Low Warning | Value is 3.0V | R | 7548 |
| 176-177 | 2 | Rx Power High Alarm | Value is 4.5dBm | R | 6E18 |
| 178-179 | 2 | Rx Power Low Alarm | Value is -16.4dBm | R | 00E5 |
| 180-181 | 2 | Rx Power High Warning | Value is 2.5dBm | R | 4577 |
| 182-183 | 2 | Rx Power Low Warning | Value is -14.4dBm | R | 016B |
| 184-185 | 2 | Tx Bias High Alarm | Value is 75mA | R | 927C |
| 186-187 | 2 | Tx Bias Low Alarm | Value is 10mA | R | 1388 |
| 188-189 | 2 | Tx Bias High Warning | Value is 70mA | R | 88B8 |
| 190-191 | 2 | Tx Bias Low Warning | Value is 15mA | R | 1D4C |
| 184-185 | 2 | Tx Power High Alarm | Value is 4.3dBm | R | 6930 |
| 186-187 | 2 | Tx Power Low Alarm | Value is -8.2dBm | R | 05E9 |
| 188-189 | 2 | Tx Power High Warning | Value is 3.3dBm | R | 5383 |
| 190-191 | 2 | Tx Power Low Warning | Value is -7dBm | R | 07CB |

**Notes:**

1.Register Type property：'R' means Read-only; 'R/W' means read or write operations are supported; 'W' means Write-only, the read result is fixed at 00(hex) .

2.Alarm and Warning threshold information can be defined according to customer requirements. Please connect us if you need.

3.When the digital diagnosis results of Temperature, Vcc, Bias Current, Tx Power and Rx Power, are exceed the limits defined at upper page 03h of A0 device, the related Interrupt Flags will be set to 1b to alert to users.

## Block-Diagram-of-Transceiver
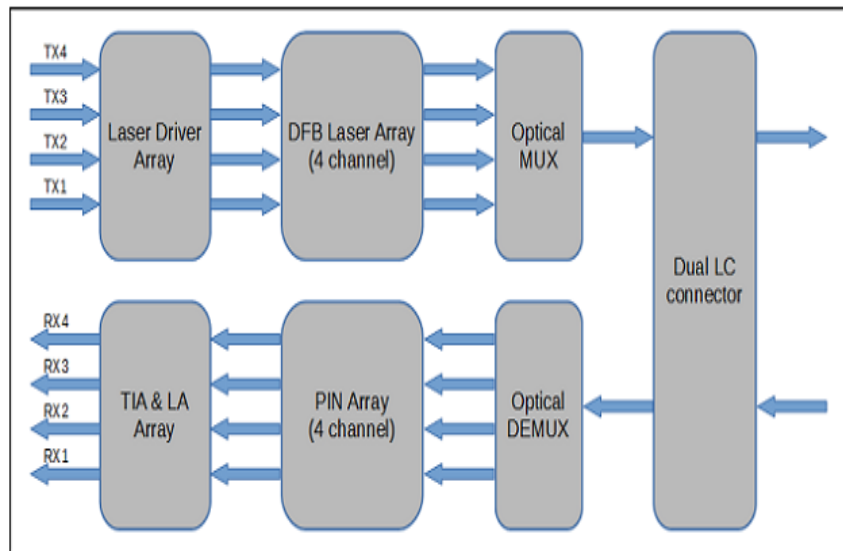


## Channel Map

| Channel (QSFP+ MSA Specification) | LAN (IEEE802.3 Specification ) | Center Wavelength |
|---|---|---|
| TX1/RX1 | L0 | 1271nm |
| TX2/RX2 | L1 | 1291nm |
| TX3/RX3 | L2 | 1311nm |
| TX4/RX4 | L3 | 1331nm |

## Functions Description

The transmitter uses 2 laser driver chips to drive a 1×4 DFB array of lasers to complete the electro-optical conversion, convert 4 10Gbps-electrical-signals to 4 CWDM-optical-signals. Optical multiplexer multiplexes the 4 CWDM-optical-signals to a 40Gbps data, which output to outside of the module through Lucent Connector.

The receiver uses a demultiplexer to demultiplex the received 40Gbps optical-signal into 4 CWDM-optical-signals.  4 CWDM-optical-signals here refers to optical signals whose center wavelengths of 1271, 1291, 1311, 1333 nm. Each wavelength of optical signals is collected by a separate photodiode and converted int a weak electrical signal. The weak electrical signal is amplified and processed by the trans-impedance amplifier (TIA) and Limiting amplifier (LA), then sent to the host.

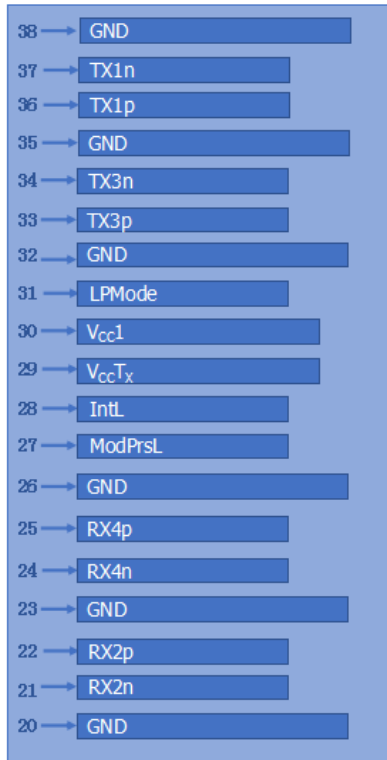There is no CDR function inside the transceiver.

## Dimensions

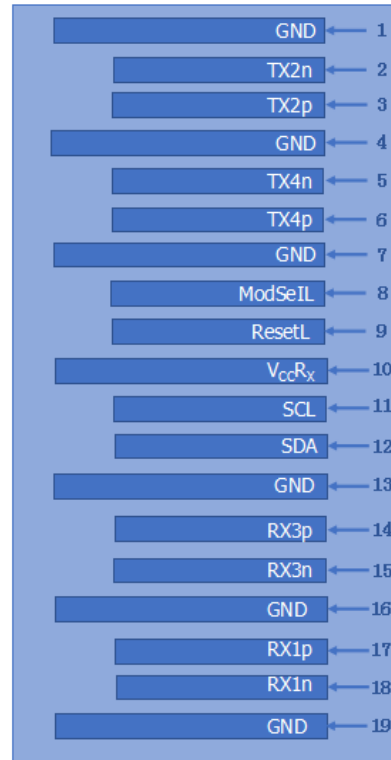Modele weight：33.4g
Dust cap weight：0.95g
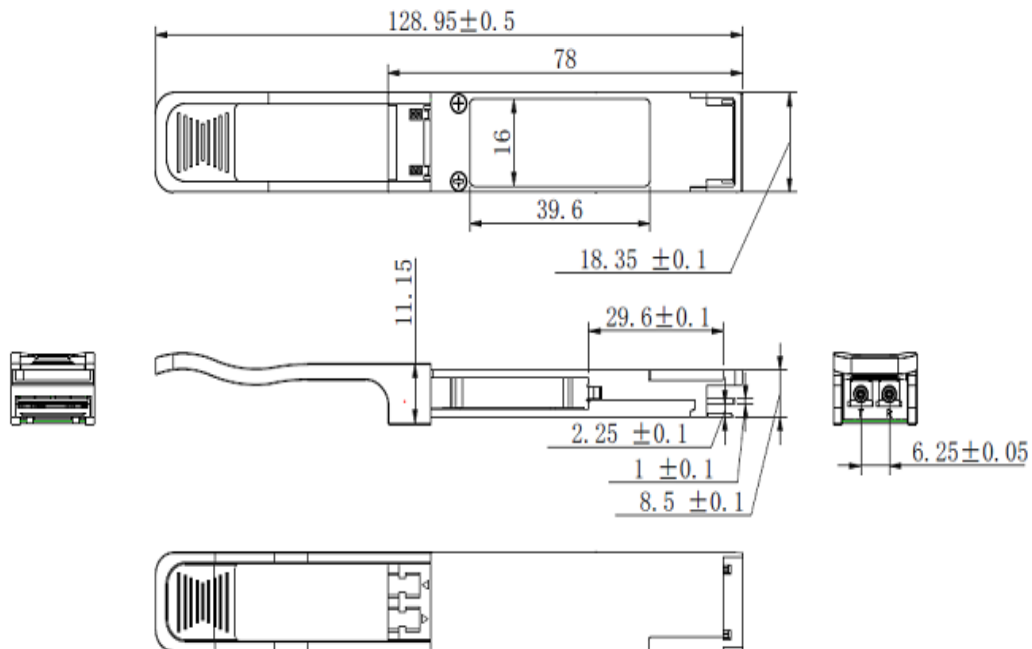
ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

## Electrical Pad Layout

| | Top of Board | | | Bottom of Board | |
|---|---|---|---|---|---|
| 38 | GND | | | GND | 1 |
| 37 | TX1n | | | TX2n | 2 |
| 36 | TX1p | | | TX2p | 3 |
| 35 | GND | | | GND | 4 |
| 34 | TX3n | | | TX4n | 5 |
| 33 | TX3p | | | TX4p | 6 |
| 32 | GND | | | GND | 7 |
| 31 | LPMode | | | ModSeIL | 8 |
| 30 | $V_{cc}1$ | | | ResetL | 9 |
| 29 | $V_{cc}T_x$ | | | $V_{cc}R_x$ | 10 |
| 28 | IntL | | | SCL | 11 |
| 27 | ModPrsL | | | SDA | 12 |
| 26 | GND | | | GND | 13 |
| 25 | RX4p | | | RX3p | 14 |
| 24 | RX4n | | | RX3n | 15 |
| 23 | GND | | | GND | 16 |
| 22 | RX2p | | | RX1p | 17 |
| 21 | RX2n | | | RX1n | 18 |
| 20 | GND | | | GND | 19 |

**Top of Board**    **Bottom of Board**

## Pin Assignment

| PIN # | Symbol | Description | Remarks |
|-------|--------|-------------|---------|
| 1 | GND | Ground | 5 |
| 2 | Tx2n | TX2 Transmitter Inverted Data Input | |
| 3 | Tx2p | TX2 Transmitter Non-Inverted Data Input | |
| 4 | GND | Ground | 5 |
| 5 | Tx4n | TX4 Transmitter Inverted Data Input | |
| 6 | Tx4p | TX4 Transmitter Non-Inverted Data Input | |
| 7 | GND | Ground | 5 |
| 8 | ModSelL | Module select pin, the module responds to two-wire serial communication when low level | 1 |
| 9 | ResetL | Module Reset | 2 |
| 10 | $V_{cc}R_X$ | +3.3V Power Supply Receiver | |
| 11 | SCL | 2-wire serial interface clock | |
| 12 | SDA | 2-wire serial interface data | |
| 13 | GND | Ground | 5 |
| 14 | Rx3p | Rx3 Receiver Non-Inverted Data Output | |
| 15 | Rx3n | Rx3 Receiver Inverted Data Output | |
| 16 | GND | Ground | 5 |
| 17 | Rx1p | Rx1 Receiver Non-Inverted Data Output | |
| 18 | Rx1n | Rx1 Receiver Inverted Data Output | |
| 19 | GND | Ground | 5 |
| 20 | GND | Ground | 5 |
| 21 | Rx2n | Rx2 Receiver Inverted Data Output | |
| 22 | Rx2p | Rx2 Receiver Non-Inverted Data Output | |
| 23 | GND | Ground | 5 |
| 24 | Rx4n | Rx4 Receiver Inverted Data Output | |
| 25 | Rx4p | Rx4 Receiver Non-Inverted Data Output | |
| 26 | GND | Ground | 5 |
| 27 | ModPrsL | The pin grounded in the module indicates the status of the module inserted into the host. When voltage level is high, the module status is inserted. | |
| 28 | IntL | Interrupt | 3 |
| 29 | $V_{cc}T_X$ | +3.3V Power Supply transmitter | |
| 30 | $V_{cc1}$ | +3.3V Power Supply | |
| 31 | LPMode | Low Power Mode | 4 |

| 32 | GND | Ground | 5 |
|----|-----|--------|---|
| 33 | Tx3p | Tx3 Transmitter Non-Inverted Data Input | |
| 34 | Tx3n | Tx3 Transmitter Inverted Data Input | |
| 35 | GND | Ground | 5 |
| 36 | Tx1p | Tx1 Transmitter Non-Inverted Data Input | |
| 37 | Tx1n | Tx1 Transmitter Inverted Data Input | |
| 38 | GND | Ground | 5 |

**Notes:**

1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module

2. The module reset pin. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) , 2 us, initiates a complete module reset, returning all user module settings to their default state. See MSA standards for related timing specifications.

3. This pin is the open-collector output pin. It shall be pulled up towards Vcc on the host board use 4.7-10 KΩ resister. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

4. When this pin is asserted high level, it indicates the module operate in low power mode and the module power consumption is lower than 1.5 Watts.

5.Circuit ground is internally isolated from chassis ground.

# References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.

2. QSFP+ 10Gbps 4X PLUGGABLE TRANSCEIVER –SFF-8436 V4.9, 2018.

3. Management Interface for 4-lane Modules and Cables –SFF-8636 Rev 2.10a, 2019.